In this paper, a thorough design procedure for concurrent design of integrated antiparallel Schottky-diode-based limiter and low noise amplifier (LNA) is presented. The optimum number of limiter branches, the size and number of diodes in each branch, width of the transmission line loaded by diode branches, and design considerations for input transistor of the LNA are discussed in detail. To improve power handling of the limiter with a minimum impact on overall noise figure (NF), a novel limiter structure is proposed where transistors are utilized in a limiter topology. A design procedure is also introduced for the transistor-based limiter-LNA. Developed methodologies are employed to design and fabricate a diode-based and transistor-based limiter-LNA in a 0.1-μm AlGaAs/InGaAs pHEMT process. Measurement results show that the diode-based limiter-LNA tolerates up to 2-W continuous wave (CW) input power without failure, while transistor-based limiter-LNA is capable of handling 5-W CW input power. Measured average gain and NF for the diode-based limiter-LNA are 21 and 2.3 dB over 28-38-GHz frequency range, while the transistor-based limiter-LNA achieves an average 18-dB small-signal gain and 2.5-dB NF over the 30-38-GHz bandwidth.