In this paper, two fully integrated digital power amplifiers (DPAs) intended for polar transmitters are proposed using a 40-nm CMOS technology, which achieve ultra wideband and high efficiency simultaneously. Firstly, the wideband Class-E power amplifier with nonideal characteristics is analyzed. Secondly, the design procedure of converting the nonideal Class-E model to a compact matching network is introduced for the on-chip implementation. Thirdly, the stacked-stepped-impedance transformer is utilized for the wideband output-matching network to improve the DPA power efficiency while tracking optimum load impedance. Finally, to enhance the saturated and back-off efficiency within a wideband, a novel feed-forward DPA architecture for a digital polar transmitter with multi-mode dynamic-matching (DM) network is firstly introduced and demonstrated. To verify the mechanism mentioned above, two DPAs are implemented and fabricated, which are the only reported wideband DPAs operating above 3 GHz with record fractional bandwidths, i.e., 92% and 100.8%, respectively. The proposed DPAs (i.e., DPA-I and DPA-II) exhibit peak output power of 22.2 and 22.3 dBm and peak drain efficiency of 46.2% and 47.4%, respectively, with a 1.2-V supply. In DM modes, the saturated and 6-dB back-off drain efficiency of DPA-II achieve maximum improvements of 7.5% and 5.7%, respectively. The core chip-sizes of the proposed DPAs (i.e., DPA-I and DPA-II) are 0.22 mm^2 and 0.24 mm^2, respectively.