Interleaving of voltage-source converter (VSC) legs enables higher output currents per phase, effectively increasing the power rating without increasing semiconductor ratings. However, the interleaved operation results in circulating currents between each phase converter legs as well as a zero-sequence circulating current (ZSCC), which become quite prominent when the converters operate with low switching frequencies. This paper demonstrates the interleaved operation of three-level converters under selective harmonic elimination pulsewidth modulation (SHE-PWM). A controller for the circulating current within the legs of each phase is also proposed. The controller is used in combination with optimally selected SHE-PWM patterns to generate the maximum number of voltage levels and minimize the peak value of the circulating current. Simulation and experimental results show the interleaved operation and the effect of SHE-PWM pattern selection in the overall system.