The complexity of narrow transition band FIR filters is high and can be reduced by using frequency-response masking (FRM) techniques. These techniques use a combination of periodic model filters and, possibly periodic, masking filters. Time-multiplexing is in general beneficial since only rarely does the technology bound maximum obtainable clock frequency and the application determined required sample rate correspond. Therefore, architectures for time-multiplexed FRM filters that benefit from the inherent sparsity of the periodic filters are introduced in this paper. We show that FRM filters not only reduce the number of multipliers needed, but also have benefits in terms of memory usage. Despite the total amount of samples to be stored is larger for FRM, it results in fewer memory resources needed in FPGAs and more energy efficient memory schemes in ASICs. In total, the power consumption is significantly reduced compared with a single-stage implementation. Furthermore, we show that the choice of the interpolation factor that gives the least complexity for the periodic model filter and subsequent masking filter(s) is a function of the time-multiplexing factor, meaning that the minimum number of multipliers not always corresponds to the minimum number of multiplications. Both single-port and dual-port memories are considered, and the involved tradeoff in number of multipliers and memory complexity is illustrated. The results show that, for FPGA implementation, the power reduction ranges from 23% to 68% for the considered examples.